

# A simple route to annihilate defects in silicon nanowires

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## Abstract

Defects inside silicon nanowires (SiNW) could be significantly reduced by annealing the nanowires at 1100° C for 6 h. High-resolution transmission electron microscopy (HRTEM) showed that stacking faults and twins were annihilated upon annealing. In particular, the tips of the nanowires demonstrated perfect lattices free of defects after annealing. Raman spectra also confirmed that the bulk specimen was almost defect-free. By using thermal annealing, defect-free silicon nanowires can be prepared in a simple and practical way, which holds promise for nanoelectronic applications. © 2000 Elsevier Science B.V. All rights reserved.

## 1. Introduction

Silicon nanowires (SiNW) have attracted much attention since large scale synthesis of SiNWs was achieved [1–3]. This achievement is mainly due to the recognition of the bulk-quantity growth mechanism of SiNWs [4–6]. The success in large scale synthesis of SiNWs has meant that research is not limited to theoretical area [7–9], but can be extended to the experimental area. To date, numerous experimental results on SiNWs have been reported, including those from transmission electron microscopy (TEM) [10,11], X-ray diffraction [2], electron transport [12], photoluminescence [13,14], infrared-induced emission [15], Raman spectroscopy [16,17], and field-emission [18]. These results have helped to speed up the study of its potential applications, since

SiNW is one of the promising materials for future nanoelectronics. However, the as-grown SiNWs typically possess a high density of defects [10,11], that would degrade their properties. Therefore, synthesis of defect-free SiNWs is of great interest.

Recently, Holmes et al. [19] obtained defect-free SiNWs, with nearly uniform diameters ranging from 40 to 50 Å and a length of several micrometers, by using a supercritical fluid solution-phase approach. However, these nanowires contained metallic nanoparticles, since gold was added as a catalyst in this method. This metallic contamination will degrade the properties of the nanowires. As we reported recently, bulk-quantities of high purity SiNWs without metallic catalyst nanoparticles can be achieved with oxide-assisted growth [4–6]. Therefore, the properties measured from this type of pure SiNWs are less affected by impurities. However, a considerable number of defects still remains inside the nanowires, as revealed by high-resolution transmission electron microscopy (HRTEM) [10,11]. In this Letter, we report that

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the defect density in SiNWs can be significantly decreased by high-temperature thermal annealing.

## 2. Experimental

The as-grown SiNWs were synthesized by the laser ablation method reported elsewhere [20]. The SiNWs were put into the middle of a quartz tube mounted inside a high-temperature tube furnace. After the pressure in the tube was pumped down to  $4 \times 10^{-3}$  Torr, argon was fed into the tube as a protective gas and the furnace temperature was increased to 1100°C for 6 h. 1100°C was used as the annealing temperature because nanowires react to become SiO vapor and disappear above this temperature [21]. During annealing, a total pressure of 740 Torr was maintained. Afterwards, small pieces of the specimen were taken off directly from the sample and mounted onto TEM grids for TEM observation. The TEM observations were carried out with either a conventional Philips CM 20 or a high-resolution Philips CM 200FEG TEM operated at 200 kV.

## 3. Results and discussion

A typical TEM image of the morphology of the annealed nanowires is shown in Fig. 1. From this image, most of the nanowires can be seen to con-

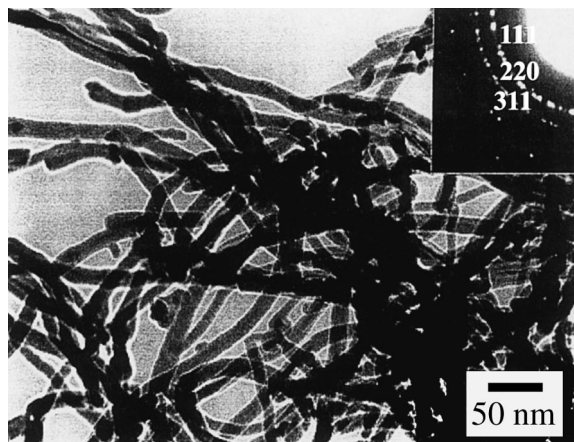


Fig. 1. TEM morphology of annealed SiNWs. The inset is a SAED pattern.

sist of straight and smoothly curved parts. The diameters of the nanowires are around 16 nm, that is almost the same as the as-grown nanowires. The inset in Fig. 1 is a select-area electron diffraction (SAED) pattern taken from the nanowires. The diffraction rings match well with the (1 1 1), (2 2 0) and (3 1 1) diffraction rings of silicon with a diamond structure. Analysis using energy dispersive X-ray spectroscopy (EDS) attached to the TEM confirmed that the nanowires have a crystalline Si core and an amorphous silicon oxide outer layer. In short, the general morphology and diameters of the annealed nanowires were the same as the as-grown SiNWs.

However, the density of defects inside the annealed nanowires decreased significantly. Fig. 2A shows the HRTEM image of a typical as-grown SiNW taken along the [1 1 2] direction. The contrast of the Si core revealed a complicated feature, indicating the presence of many defects. Stacking

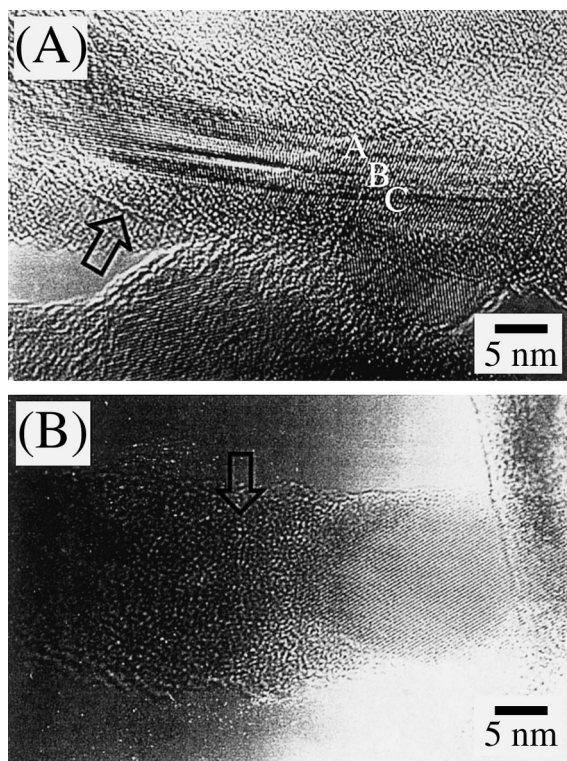


Fig. 2. Typical HRTEM images of SiNWs: (A) an as-grown SiNW with defects; (B) an annealed SiNW without defects.

faults on the (1 1 1) plane appearing in the form of narrow bands (marked A, B, C) lying along the [1 1 2] growth direction of the nanowire can be clearly observed. An arrow points to the edge of the nanowire. After annealing, the defect density in the nanowires was much lower, as shown in Fig. 2B. The amorphous surface of the nanowire (indicated by the arrow) can also be seen clearly, since it falls in the same focus plane of the Si core. It should be pointed out that investigation was carried out on a statistical sampling of SiNWs, so that the HRTEM images shown in Figs. 2 and 3 (below) of the annealed nanowire are representative morphologies.

Defects in the tips of SiNWs were also annihilated. The tip of an as-grown nanowire is shown in the HRTEM image in Fig. 3A. The tip is generally hemispherical in shape and covered by a relatively thick amorphous silicon dioxide layer. The contrast of the amorphous layer was quite uniform and only the Si crystalline structure was observed within the tip. Similar to the microstructure in the body of the nanowire, the Si crystal core in the tip also has a high density of stacking faults and micro-twins, along the axis of the nanowire in the [1 1 2] growth direction (indicated by the arrow). In our observation, this is a common phenomenon in the tips. The presence of these defects in the tip areas is considered to be responsible for the fast growth of SiNWs, since it is well known that dislocations can accelerate crystal growth. In other words, the defects in the tips of SiNWs are necessary for the growth of SiNWs. However, the tips of the annealed nanowires demonstrate perfect lattices because the defects in the tips have been annihilated, as shown in Fig. 3B. The arrow points to the [1 1 2] growth direction of the nanowire. Considering that carbon nanotubes have been used as good nanoprobe [22], the nanowires with sharp tips and perfect lattices might also be promising materials for future nanoprobe.

Defects in the bulk samples were further studied with Raman spectroscopy. Fig. 4 shows the Raman spectra of the as-grown SiNWs [spectrum (a)], the annealed SiNWs [spectrum (b)] and the reference single crystalline Si wafer [spectrum (c)]. The as-grown SiNWs shows a Raman peak with high asymmetry while the annealed SiNWs gives a more

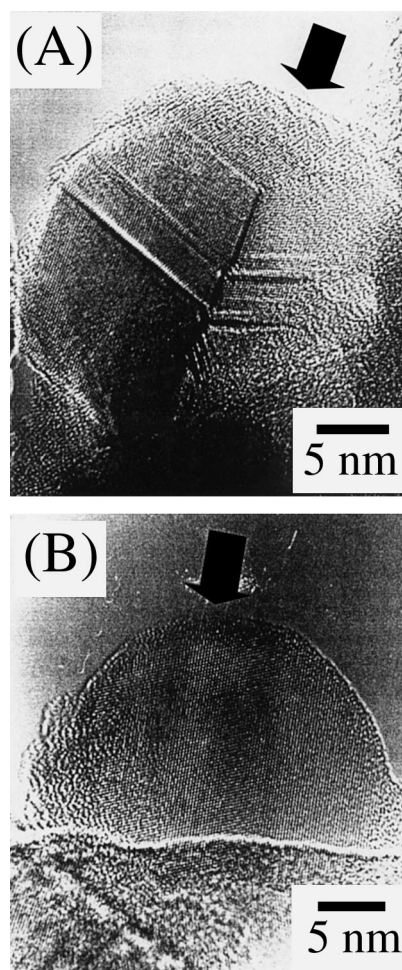


Fig. 3. Typical HRTEM images of the tips of SiNWs: (A) the tip of an as-grown SiNW with defects; (B) the tip of an annealed SiNW with a perfect lattice.

symmetric peak. The asymmetry of the Raman peak is contributed to by two factors: nanoscale size and defects [23,24]. In the present experiment, the diameters of the nanowires do not change upon thermal annealing, which can be seen in Fig. 1. Moreover, the shifts of spectra (a) and (b) due to the size effect [25] are the same. Thus, we conclude that the decrease in peak asymmetry is attributed to the decreasing density of defects. It should be noticed that the signal-to-noise ratio in spectrum (b) is much less than that in spectrum (c). As a result, the small ratio may have increased the asymmetry in spectrum (b). Therefore, the defects in the

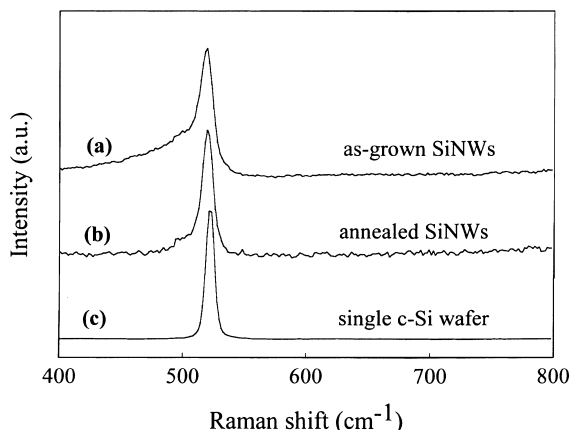


Fig. 4. The Raman spectra of: (a) as-grown SiNWs; (b) annealed SiNWs; (c) a reference single c-Si wafer.

nanowires [spectrum (b)] are much less than what appears in the spectrum, and may even be comparable to the single crystalline Si wafer [spectrum (c)].

#### 4. Conclusions

In conclusion, the defects inside the SiNWs were significantly decreased after the SiNWs were thermally annealed at 1100°C for 6 h under an inert ambient. HRTEM investigation of the microstructures in the nanowires after annealing showed that stacking faults and micro-twins in the as-grown Si nanowires were annihilated. Raman studies confirmed that the whole annealed sample consisted of low defect density. The SiNWs with low defect density are promising materials for nanoelectronic applications.

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